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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/879,724	06/12/2001	Dong-Hyuk Ju	F0522	4898
7590	04/10/2002			<i>HC</i>
			EXAMINER	
			SEFER, AHMED N	
		ART UNIT	PAPER NUMBER	
		2826		
DATE MAILED: 04/10/2002				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/879,724	JU ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 19 February 2002.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) 11-16 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-10 and 17 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ . | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I in Paper No. 3 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 112

2. Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 1 recites the limitation "the polysilicon layer". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-10, as they are understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Begley et al. US Patent No. 5,773,151.

Begley et al disclose (see fig. 8 and col. 1, lines 58-62) a semiconductor-on-insulator (SOI) structure having a semiconductor substrate 85 or silicon (as in claim 2); a leaky, thermally conductive insulator material (LTCIM) layer 84 with a thermal

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value of about 30 W/mk to about 170 W/mk (as in claim 3) or silicon (as in claim 4) with a resistivity value 10 Ω-cm or greater (as in claim 5) or undoped single crystalline silicon (as in claims 6 and 7) or undoped porous silicon (as in claims 8 and 9) or amorphous silicon (as in claim 10) disposed on the semiconductor substrate; and a semiconductor layer 88 disposed on the LTCIM layer; and active region defined in the semiconductor layer by isolation trenches and the polysilicon layer.

6. Claims 1-7, as they are understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Sugiyama US Patent No. 5,637,513.

Sugiyama discloses (see fig. 9 and col. 9, lines 41-50 and claims 8 and 14) a semiconductor-on-insulator (SOI) structure having a semiconductor substrate 11 or silicon (as in claim 2); a leaky, thermally conductive insulator material (LTCIM) layer 19 with a thermal conductivity value of about 30 W/mk to about 170 W/mk (as in claim 3) or silicon (as in claim 4) with a resistivity value 10 Ω-cm or greater (as in claim 5) or undoped single crystalline silicon (as in claims 6 and 7) disposed on the semiconductor substrate; and a semiconductor layer 13 disposed on the LTCIM layer; and active region defined in the semiconductor layer by isolation trenches and the polysilicon layer.

7. Claims 1-10, as they are understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Takenori (JP 7-86298)

Takenori discloses in fig. 8 a semiconductor-on-insulator (SOI) structure having a semiconductor substrate 1 or silicon (as in claim 2); a leaky, thermally conductive insulator material (LTCIM) layer 3 with a thermal conductivity value of about 30 W/mk to about 170 W/mk (as in claim 3) or silicon (as in claim 4) with a resistivity value 10 Ω-cm

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or greater (as in claim 5) or undoped single crystalline silicon (as in claims 6 and 7) or undoped porous silicon (as in claims 8 and 9) or amorphous silicon (as in claim 10) disposed on the semiconductor substrate; and a semiconductor layer 5 disposed on the LTCIM layer; and active region defined in the semiconductor layer by isolation trenches and the polysilicon layer.

8. Claims 1-3, as they are understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Linn et al. US Patent No. 5,569,620.

Linn et al disclose in fig. 6 a semiconductor-on-insulator (SOI) structure having a semiconductor substrate 612 or silicon (as in claim 2); a leaky, thermally conductive insulator material (LTCIM) layer 615,613 with a thermal conductivity value of about 30 W/mk to about 170 W/mk (as in claim 3) disposed on the semiconductor substrate; and a semiconductor layer 602 disposed on the LTCIM layer; and active region defined in the semiconductor layer by isolation trenches and the polysilicon layer.

9. Claims 1-3, as they are understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Yamaguchi et al. US Patent No. 5,777,365.

Yamaguchi et al disclose in fig. 2 a semiconductor-on-insulator (SOI) structure having a semiconductor substrate 1 or silicon (as in claim 2); a leaky, thermally conductive insulator material (LTCIM) layer 16 with a thermal conductivity value of about 30 W/mk to about 170 W/mk (as in claim 3) disposed on the semiconductor substrate; and a semiconductor layer 3 disposed on the LTCIM layer; and active region defined in the semiconductor layer by isolation trenches and the polysilicon layer.

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10. Claims 1-3, as they are understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Schrantz et al. US Patent No. 5,561,303.

Schrantz et al disclose in fig. 5 a semiconductor-on-insulator (SOI) structure having a semiconductor substrate 10 or silicon (as in claim 2); a leaky, thermally conductive insulator material (LTCIM) layer 12 with a thermal conductivity value of about 30 W/mk to about 170 W/mk (as in claim 3) disposed on the semiconductor substrate; and a semiconductor layer 32 disposed on the LTCIM layer; and active region defined in the semiconductor layer by isolation trenches and the polysilicon layer.

11. Claim 17 is rejected under 35 U.S.C. 102(b) as being anticipated by Linn et al. US Patent No. 5,569,620.

Linn et al disclose in fig. 6 a semiconductor-on-insulator (SOI) structure having a semiconductor substrate 612; a leaky, thermally conductive insulator material (LTCIM) layer 615, 613 disposed on the semiconductor substrate; and a semiconductor layer 602 disposed on the LTCIM layer; a gate defining a channel interposed between a source and a drain formed within an active region of the SOI structure; and the active region defined in the semiconductor layer by isolation trenches and the LTCIM layer.

12. Claim 17 is rejected under 35 U.S.C. 102(b) as being anticipated by Schrantz et al. US Patent No. 5,561,303.

Schrantz et al disclose in fig. 5 a semiconductor-on-insulator (SOI) structure having a semiconductor substrate 10; a leaky, thermally conductive insulator material (LTCIM) layer 12, 40 disposed on the semiconductor substrate; and a semiconductor layer 32 disposed on the LTCIM layer; a gate defining a channel interposed between a

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source and a drain formed within an active region of the SOI structure; and the active region defined in the semiconductor layer by isolation trenches and the LTCIM layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (703) 308-6601.

ANS
March 29, 2002

A handwritten signature in black ink, appearing to read "AS", is positioned above a typed name and date.